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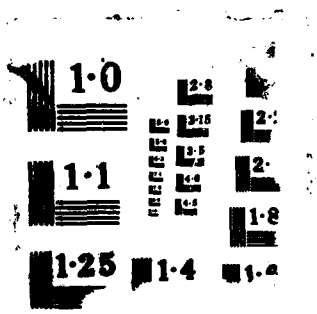
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ROYAL SIGNALS AND RADAR ESTABLISHMENT

Memorandum 4143

Title PRACTICAL CUSTOM CMOS CHIP DESIGN

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Date MAY 1988

Summary

Customised or Application Specific ICs (ASICs) are being used increasingly as designers appreciate their benefits and its cost has reduced dramatically with the progress of CAD and processing technology. After a brief discussion of the benefits of the custom chip design route, the steps involved in the design cycle are outlined with particular emphasis on the practical aspects involved in translating circuit ideas to working silicon.
Shared-wafer silicon services have reduced significantly the cost of Full-custom chips and some practical experiences of Full Custom CMOS chip design are outlined. The design, simulation and layout were all carried out at RSRE. The work was undertaken as part of a research program on novel cell architectures for DSP VLSI chip design within SP2.

Sections

Tables

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1 Introduction

The traditional view that custom ICs cannot be considered unless there is a requirement for at least hundreds of devices no longer holds true.

IC process technology and design systems to make ready use of the advanced processes have made significant progress over the last few years. This has meant that custom ICs are very much easier to specify and procure and that they are cost effective in a wide range of projects.

In the next section we classify and describe the various routes to silicon for custom ICs. Section 3 outlines the advantages to be gained from the use of custom chips. Section 4 describes the various levels of system specification, while section 5 outlines the design cycle for custom ICs. Sections 6 to 9 cover various aspects of the use of the full-custom design route, which we have used in our research program. Section 6 outlines the shared-wafer device fabrication services, which have reduced the cost of the full-custom route to silicon. In section 7 we show how a transistor level circuit is translated into a IC layout. Section 8 details some of the features of the Computer aided design system we have used. While section 9 gives an overview of the full-custom chip produced. In the final section we present some conclusions.

2 Routes to Silicon

The cost of and the time to procure semi custom and full custom ICs has reduced dramatically, to the extent where it should be considered by any designer requiring even a one-off system that uses a few tens of standard logic ICs. This is due to the continuing advances in Computer aided design and process technology. These factors have significantly changed the picture with regard to the options available to potential users of IC systems.

There are three basic classes of custom IC, dependent on how much additional processing has to be carried out on the silicon chips. The table below shows these classes, in order of cost.

Class	Level of integration	Cost	Additional silicon processing steps
PLD	MSI - LSI	Low	None
Gate Arrays	MSI - VLSI	Low - High	Final metal layers
Full Custom	LSI - ULSI	Medium - Very High	Full mask set

Table 1 classes of custom ICs

The relative positions can change depending on the process technology available. Also the software to describe and simulate the IC will have a significant impact on the overall design cycle.

For all of these approaches libraries of standard functions are made

available in the design software, what differs is how these functions are actually implemented on the IC. In the following paragraphs we describe these differences and give some general details about each approach.

2.1 Programmable Logic Devices (PLD)

This term is used to cover a broad range of devices all of which have the ability to be customised without any additional silicon processing steps. This means that custom ICs can be generated in a matter of hours or days rather than weeks for gate arrays or months for the full-custom options. **Programmable logic arrays** are a very convenient way of mapping irregular logic functions onto a regular structure. This regularity makes them easy to fabricate. They consist typically of programmable AND-OR arrays. The customisation of the arrays being carried out by blowing of fuse links or more recently the down-loading of a configuration program into static on-chip memory. The latest PLDs are electrically reprogrammable gate arrays, these offer up to 9000 gate capability.

Applicability Electrically Programmable Logic Devices (EPLDs) are ideal for low volume prototype systems where continual development and upgrading can be readily accommodated. Prices range from £20 to £250 depending on capacity. Xilinx and Altera are two of the major players in this field. EESD at RSRE have a development system for the Xilinx products.

2.2 Gate arrays

Gate arrays (or ULAs uncommitted logic arrays) are regular arrays of small groups of transistors which have been preprocessed up to the final metal interconnect and routing layer(s). In conventional gate arrays the predefined groups of transistors can be turned into various logic functions using the final metal layers. Groups of these gates can be connected together to give the required function, so with these devices some additional processing steps are required.

A bewildering variety of products are available offering gate counts from under 1000 to over 100,000. It should be noted that there will be a significant difference between the quoted gate count and that actually obtainable in a practical design. Usable gates will be in the range 40% to 75% of the stated figure. Prices for state-of-the-art, very large arrays are upwards of £50,000 which would preclude their use in all but the most advanced prototype or system demonstators. However there have been some very interesting developments at more modest integration levels.

MCE at Tewkesbury are offering their Falcon service, which is a shared project gate array service offering prototype quantities on a 1440 gate array for £600. The design software is available for IBM PCs or VAXs at a cost of £600. They have recently intoduced a 2500 gate array service for £2500. The turn around times for designs can be quite short with regular (monthly) production runs. EESD have the design and simulation packages.

Applicability The shared project gate array design route should be considered when there is a fixed design with the need for a minimum chip count and the possibility of requiring a few tens off in the near future.

There have been recent developments in the gate array market to merge together Bipolar and CMOS processes to give the BICMOS process. This offers the speed and drive capability of Bipolar along with the integration levels and low power of CMOS. This approach also offers the ability to combine analogue and digital functions on the same chip. Various gate arrays with analogue and digital sections on them are available.

2.3 Full-Custom chips

Full-custom has no predefined patterns on the silicon, the designer either has to define his own cells at the mask level or make use of the full-custom standard cells available from the vendor. A full mask set has to be generated. The ultimate levels of integration can potentially be achieved using **Full-Custom** design, but the time and cost involved in handcrafting each portion of a large IC means the task would be unmanageable for most ICs.
This design task can be reduced significantly by the use of **Standard Cells**, various predefined and optimised cell layouts, such as latches, gates, etc. These cells can have either been defined as gate array type structures (to give the so called compacted gate arrays) or as handcrafted cells which will offer optimum circuit size and performance. The Full custom approach offers increased integration levels, but has traditionally resulted in a higher cost due to the need to produce a full mask set. However this has changed with the advent of the shared-wafer processing services. These will be discussed in section 6.

Applicability for certain classes of ICs with regular architectures (in particular some classes of Digital Signal Processing ICs). Also when the optimum size and power are required.

3 What are the advantages of IC chip design ?

There is a range of advantages to be gained from the integration of a system or circuit design using one of the approaches described in the previous section.

Improved system performance - greater throughput rate, lower power consumption, due to the reduction of the number of 'off chip' interconnects (which require large,power consuming line drivers).

Significantly reduced system size - reduced component count gives a higher packing density.

More reliable system, interconnections and plugs and sockets are relatively unreliable - reduction of the number of these interconnects increases system MTBF.

Increased design security - more difficult to reverse engineer.

4 System Specification of Custom ICs

One of the most important aspects of custom IC design is the need for a precise specification of the system to be implemented. This is used as the reference when making checks to validate the design of the system.The specification can be written using one of the Hardware description languages (HDLs) or may be entered in schematic form. The system may be specified at a range of levels of description, the most appropriate starting point depending on the system complexity. The table below shows the various levels. For small chips the most useful initial description level is gate level. However we breifly describe the behavioural level for completness.

Level	Feature described	Technology dependence
Behavioural	Black box	Independent
Functional	Register/gate	Implicit
Physical	Layout	Specific

Table 2 levels of system specification

The initial system concept or circuit idea can be turned into a high level description of the system, the behavioural description. At this level modules that make up the system and the control and communication paths between them are specified but there is no indication as to how this is achieved.

The next level down this heirarchical description of the system is the one most commonly used in conventional standard logic system design. At the functional level the nature of the signals at any point are known as are the bus widths. The nature of the modules are specified down to the gate level so there is an implicit technology dependence, as particular technologies can be very effective at implementing specific types of gates.

The lowest level is the physical specification. This details the layout at the transistor level description of the circuit.

There is a broad range of descriptions, even within each level of specification. This diversity is illustrated by a simple example of a 4bit binary adder. The adder can be described either schematically, as in figure 1 or in textual form.

4.1 Behavioural description

At the behavioural level (figure 1a) the form of the two input and one output numbers is not specified, simply that they will be added together, so in a high level language we would have

```
Result = A + B
```

We will use the ELLA hardware design and description language to illustrate the range of functional descriptions available to system designers. At its highest level ELLA uses ARITH statements,that allow

one to describe hardware processes without describing how these processes will be implemented. For example the statement

```
FN ADD = (int : a b) -> result : ARITH a + b .
```

defines a module called ADD which takes in two integers a & b and produces the result (a+b) in integer form. If it were not for the fact that the values have to be integer this could be considered behavioural.

4.2 Functional description

The functional level encompasses a wide range of descriptions. At the register level we describe fully the logic signals and the allowed states of the register. Figure 1(b) shows the ADD module being implemented with four 1-bit full adder modules, these are connected together giving a 5bit result . We can describe this BITADD function as a truth table, without giving any indication as to how the implied functionality will be achieved.

```
      FN BITADD = (bool: a b cin) -> (bool,bool):
CASE (abit,bbit,cbit) OF (f,f,f) -> (f,f),
       ((t,f,f)|(f,t,f)|(f,f,t)) -> (t,f),
       ((t,t,f)|(t,f,t)|(f,t,t)) -> (f,t),
                         (t,t,t) -> (t,t) ESAC.
```

The gate level description is the most commonly used in circuit design (figure 1c). The ELLA description shows BITADD taking 3 boolean values as inputs a,b,cin and delivering two boolean outputs, the sum and carry. The MAKE statements generate the instances of the gates (previously defined in a user library), so INV is a standard inverter, with two instances in the bitadder, inv1 and inv2. The JOIN section of the program describes the connections between the various gates.

```
FN BITADD = (bool: a b cin) -> (bool,bool):
BEGIN
          MAKE TWO_OR : two_or1,
             THREE_OR : three_0r1,
              TWO_AND : two_and1 two_and2 two_and3,
              TWO_NOR : two_nor1 two_nor2,
            THREE_AND : three_and1,
                  INV : inv1 inv2.

          JOIN (a,b) -> two_or1,
               (a,b) -> two_and1,
      (two_or1,cin) -> two_and2,
 (two_and2,two_and1) -> two_nor1,
           two_nor1 -> inv1,

           (a,b,cin) -> three_or1,
           (a,b,cin) -> three_and1,
  (three_nor1,two_nor1) -> two_and3,
(two_and3,three_and1) -> two_nor2,
           two_nor2 -> inv2.
 LET cout = inv1 , sout = inv2.
 OUTPUT (cout,sout)
 END
```

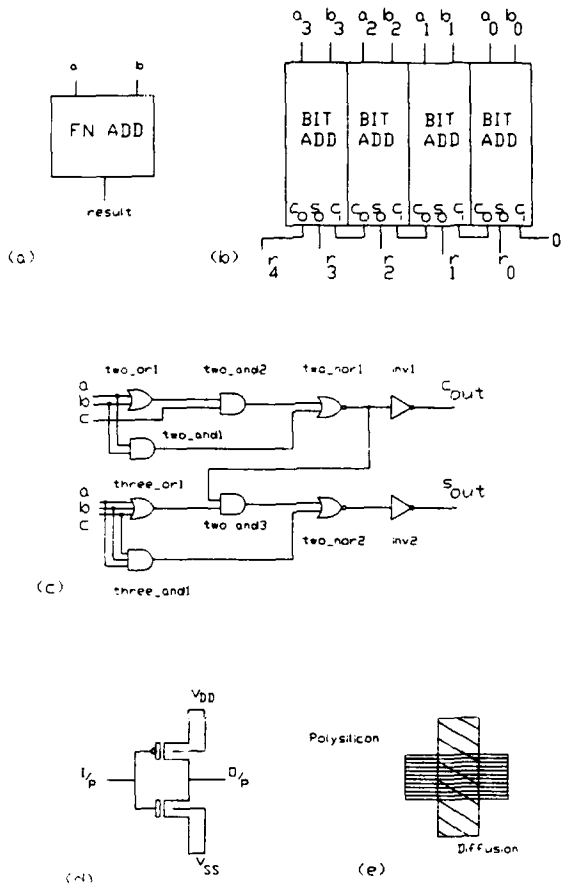

Figure 1 Hierachical specification of adder

One can see that the amount of program text used to describe the circuit increases greatly the further down the chain we go.

The lowest level of functional description is the transistor (or switch) level, the form at this level is shown in figure 1d, for the simplest gate in the circuit,the inverter.

4.3 Physical description

At the physical level we are looking at the nature of the various mask layers that are used to define physically the transistors and interconnects used in the circuit, figure 1e shows the simplest form of this, with polysilicon crossing over diffusion to define a transistor. There are various standards to describe the different layers used in the fabrication of ICs, these include GDS II, CIF and EDIF.

5 The design cycle for custom ICs

The design cycle for any custom IC will differ slightly from the conventional standard logic route in that it will impose a rather more formal design path on the engineer. This is due mainly to the fact that it can be much more costly and time consuming to redesign and produce custom ICs if the design is in error. For this reason much time is spent in trying to ensure that the design is right first time. Figure 2 shows the main steps of the design procedure cycle.

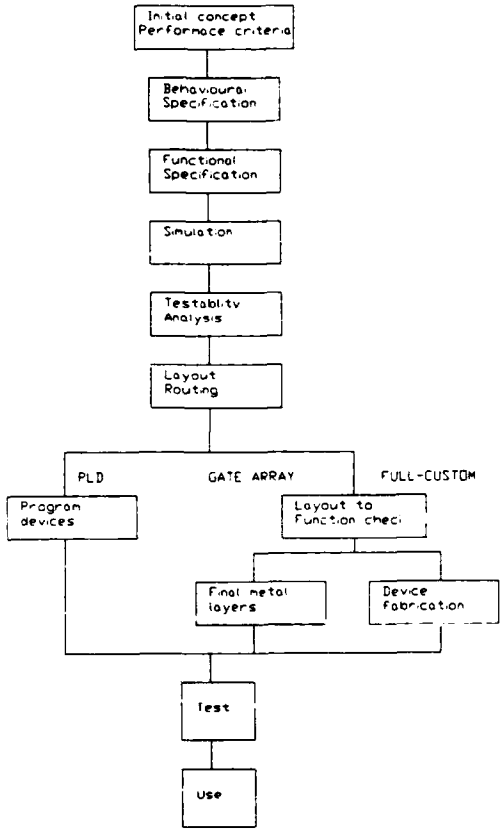

Figure 2 The Design Cycle

5.1 System specification

For very large systems the behavioural specification is taken along with some performance criteria eg. what speed is required, how much power may it consume, what sort of physical and electrical environment will it be placed in, and an initial decision is made on what technology and route to silicon is most appropriate.

A functional specification is then generated. For existing designs ie. where a gate level description already exists, this is an appropriate entry point.

5.2 Simulation

The functional level specification is then used as the basis for simulation of the system to ensure that it is logically correct and will meet the performance criteria. Essentially this is the software equivalent to breadboarding giving a 'softboarded' system.

5.3 Design for testability

Once the circuit's functionality has been proven it is then analysed to see if it can be sensibly tested, this is particularly important for any custom IC. As the design complexity increases the system must be designed with ease of testability as a major consideration. The two main factors in 'design for testability' are the controlability - the ability to set the system to known initial states, and observability - the ability to monitor the systems internal states during test. It may be necessary to include extra circuitry in the design in order to ease the task of testing the chips.

5.4 Routing and Layout

The circuit can now be 'laid out' on the target route to silicon. For example, with a gate array the circuit diagram is usually automatically mapped onto the gate array structures by the design system software, with some manual intervention if there are any awkward paths (there usually are). The layout imposed (or chosen) will put in additional capacitive loading effects, which might change the system performance, so the circuit is normally resimulated with these effects taken into consideration.

6 Shared wafer silicon services

While the full custom design route offers the greatest level of integration, it has in the past been the most difficult route to take both in terms of time and money. But during the last three to four years some significant developments have been taking place to ease this situation. These started in the USA and have spread to the UK and Europe. In an effort to make fullest use of their very expensive silicon fabrication lines some US process houses decided to offer a multi-project full custom IC service. Basically this combined a number of different customer designs (typically 10) onto one mask set. Mask sets are expensive (£10K), so that sharing the mask costs had a very significant impact on the overall chip cost. This approach combined with the lowering cost of engineering workstations and design software has meant that the full-custom route to silicon has now become an effective way of producing demonstrator ICs.

In mid 1985 Micro Circuit Engineering Ltd (MCE) started a 3 year Alvey contract with the aim of providing a fast and low cost route to prototypes for full custom and semi custom VLSI designs on a range of multi-sourced processes. This service has been operating successfully for the past couple of years.
Initially this was for a CMOS 3µm P-well single- and double-layer metal processes with access to AMI, MITEL, EUROSIL, ORBIT, and TI. They have recently added 2µm CMOS design rules with access to AMI, IMP, VTI, STC and ES2.
MCE also have a 3µm Standard Cell library along with a complete software suite covering schematic capture, hardware description language, logic simulation with test and waveform generation, so they can offer a complete design and production service if required.

There are other companies in the UK offering similar services. Integrated Circuit Design Centre Ltd offer access to and design systems for a multi-project service with 2µm CMOS.

7 Full Custom CMOS

7.1 Standard Cells

The full custom route, while offering the highest levels of system integration, requires the most time and resources to implement, but has the greatest benefit in terms of overall system performance. The design effort can be reduced by the use of a Standard Cell Library. This gets round the need for the very detailed design and simulation work involved in building your own library, as the cells have already been layed out and electrically characterised.

7.2 Crafted Cells

For most applications, the use of standard cells will produce an acceptable chip design. However in some designs, it may be necessary to acheive a highly compact circuit and in such cases the handcrafting of the entire circuit could be carried out. This requires a knowledge of how the various gates and logic functions are constructed at the transistor level and how to translate this transistor level description of the circuit into a series of geometric patterns on a set of masks that define the shapes of the different materials used in the fabrication of the transistors and other devices available in the CMOS process.

In a typical CMOS process (single layer metal), the circuit is laid out using typically 8 layers, each of which represents either a material or a process step to be carried out. The patterns on each layer are defined by a mask which is used in the fabrication of the device. Table 3 lists these design layers for the CMOS p-well process we have used.

Design Layer		Comment
number	name	
1	Diffusion Island	Outside of these areas isolating field oxide is formed.
2	P-wells	Defines lightly doped P- areas N channel devices formed in these areas.
3	Polysilicon	Forms transistor gates and local interconnect.
4	N+ Diffusion Implant	N+ sources and drains, diffusion islands within these areas receive N+ doping.
5	P+ Diffusion Implant	P+ sources and drains, diffusion islands within these areas receive P+ doping.
6	Contacts	Defines holes in oxide down which metal contacts diffusion or polysilicon.
7	Metal 1	For low resistance interconnect between components.
8	Vias	Layers 8 & 9 not used in single metal process.
9	Metal 2	
10	Passivation	Defines holes in the area of protective glass.

Table 3 CMOS process design layers

7.3 Full-custom Layout

The simple inverter gate shown in figure 3(a) is used to illustrate how the gates are turned into circuits on the silicon chip.

Basically all the power rails will be in metal. Interconnections will be metal if they are long or in polysilicon if they are local. Diffusion areas are normally too resistive for use as interconnect. Transistors are formed when a polysilicon area crosses over an implanted diffusion area.

So from figure 3(b) we can clearly identify the two transistors used in the inverter, P-channel devices are formed on the N^- subtrate, while N channel transistors are formed in the P^- well. The contact rectangles define where holes will be etched into the insulating oxide areas, so that contacts may be made between the metal and diffusion or polysilicon, a string of small contacts being more effective than a large contact.

The two contact holes in the N^+ region to the left of the P transistor drain forms an ohmic (N^+ to N^-) substrate contact, which ensure that the substrate is kept at a well-defined potential and that parasitic resistances are reduced, this helps to reduce sensitivity to 'latchup' (the switching on of parasitic bipolar transistors) which can cause irreversible damage to CMOS ICs.

A similar substrate contact is used for the N channel device, with a P^+ area making good ohmic contact from Vss to the Pvell. Figure 3(c) shows a cross-sectionional view of the construction of the inverter.

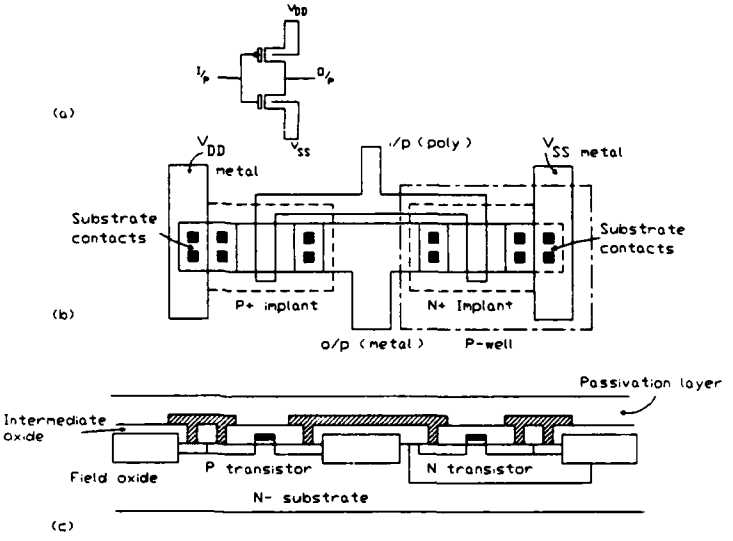

Figure 3 CMOS inverter layout

7.4 Cell characterisation

It is normal practice at this level of design to partition the layout into small groups of transistors (<30) that form functional blocks. These can then be electrically characterised by detailed circuit analysis. Although we are dealing with digital IC circuits, whose operation is normally thought off as binary valued, at this level of design we have to treat there operation as analogue.

There are many transistor level circuit simulators available but most are variants of the Simulation Program with Integrated Circuity Emphasis, more commonly known as SPICE. This program performs operating point analysis and time domain analysis.

If the circuit operation is critical then an initial simulation based on the transistor level circuit diagram would be carried out, to see if the performance is in the right ballpark, followed by a layout of the circuit to estimate the parasitic resistances and capacitances. The parasitic components are then incorporated into the final SPICE simulation to see if the circuit still meets the required performance.

An example of a simple CMOS inverter circuit described using SPICE is shown in figure 4. The inverter is operating from a 5V supply across the two transistors (M1 is a p channel and M2 is a n channel). A 5V input pulse has been defined with a period of 4μs, this is applied to the commoned gates. The node numbers in the transistor statements refer to the Drain, Gate, Source and Bulk (or substrate) connections respectively, L and W are the physical size of the transistor in microns. In the MODEL statements some of the process parameters have been shown, for example the threshold voltage, the gate oxide thickness and the transistor mobilities. The TRANS command calls for a transient analysis from 0 to 10μs with a step size of 100ns. The results of this are plotted with the input and output nodes being monitored.

```
CMOS INVERTER
.OPTIONS NOPAGE NOMOD
VDD 3 0 DC 5
VIN1 1 0 PULSE( 0 5 100NS 10NS 10NS 1.98US 4US )
M1 2 1 3 3 MOD2 L=3U W=7U
M2 2 1 0 0 MOD2 L=3U W=7U
.MODEL MOD1 PMOS LEVEL=2 VTO=-0.80 TOX=47E-9 UO=200
.MODEL MOD2 NMOS LEVEL=2 VTO=0.80 TOX=47E-9 UO=624
.TRAN 100NS 10US
.PLOT TRAN V(1) V(2) 0 5
.END
```

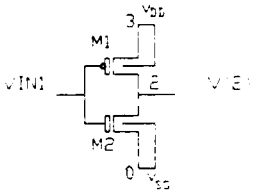

Figure 4 SPICE description of inverter

In our research work we are looking at Digital Signal Processing (DSP) IC architectures, in particular at a class of devices called bit-level systolic arrays which perform functions such as FIR filtering, convolution and correlation. Bit-level systolic arrays are highly regular arrays of 'simple' cells (typically < 100 transistors). Optimisation of these simple cells in terms of size, power and speed will have a direct impact on the performance of the whole VLSI chip (a comparison may be made with the time and effort put into the research and development carried out on memory cells). We need the total flexibility that full custom design approach offers to enable us to try out new design approaches to implement our required functions and develop higher performance DSP ICs.

8 Computer aided design (full-custom)

As can be seen from the very simple example of the inverter circuit there is quite a lot of information required to define the physical structure. For any practical system design, computer aided design (CAD) is essential to keep track of and enable the layout designer to place and manipulate the geometric patterns that define the circuit.

This section outlines the full-custom IC layout package we have made use of at RSRE. EESD has Calma's GDSII workstations running a software IC layout package called CustomPlus, this is a hierarchical, menu driven symbolic full-custom IC layout system, the layout can be approached from a top-down or a bottom-up viewpoint.

Top-down design is carried out when initial estimates of the major circuit elements and any buses between them are carried out to give an overall floor-plan for the chip. Bottom-up design is carried out by the IC layout designer when implementing the detailed circuit design for example a half latch may be designed as a basic storage element, this can be replicated to form a shift register. We also have a layout compaction program SpacerII which can be used to optimise the spacing between the various cells in the chip.

CustomPlus can be used to produce layouts for a wide range of IC processes, the different design rules and set up imformation being stored in technology bases. These technology bases hold data on the material names and some of the design rules. The design rule information is held in tables defining the minimum widths and spacing of the materials used and some properties of the layers. Table 4 shows part of the Spacing Rule File (SRF) for the system we have set up.

Design Rule Matrix

Material	L	M	W	Design Rules					
				SYMB	PERI	ISLA	PWEL	POLY	NPLU
SYMBOL	53	0	0.	40.	0.	11.	11.	3.	X
PERIMETER	54	0	0.	0.	0.	0.	0.	0.	0.
ISLAND	1	0	4.	11.	0.	6.5	11.	1.5	X
PWELL	2	0	7.	11.	0.	11.	X	X	X
POLY	3	50	3.	3.	0.	1.5	X	3.	X
NPLUS	4	50	9.	X	0.	X	X	X	X
PPLUS	5	50	9.	X	0.	X	X	X	X
CONTACT	6	0	3.	40.	0.	3.	X	X	X
METAL	7	0	4.	4.	0.	4.	X	X	X
GLASS	10	0	115.	40.	0.	X	X	X	X

Design Rule Matrix

Material	L	M	W	Design Rules			
				PPLU	CONT	META	GLAS
SYMBOL	53	0	0.	X	40.	4.	40.
PERIMETER	54	0	0.	0.	0.	0.	0.
ISLAND	1	0	4.	X	3.	4.	X
PWELL	2	0	7.	X	X	X	X
POLY	3	50	3.	X	X	X	X
NPLUS	4	50	9.	X	X	X	X
PPLUS	5	50	9.	X	X	X	X
CONTACT	6	0	3.	X	3.	X	40.
METAL	7	0	4.	X	X	4.	X
GLASS	10	0	115.	X	40.	X	X

Table 4 CustomPlus spacing rules file

CustomPlus allovs the designer to define cells which may be as simple as a single transistor or as complex as necessary. There are two basic types of cells, a rigid cell (RCELL) and a programmable cell (PCELL). RCELLS are very simple to construct but may prove to be inflexible. Any instance of an RCELL in a circuit layout looks identical to the original, although tricks can be played to modify the size of different parts of the cells.

PCELLS are much more flexible, but require a significantly greater design effort to implement them. Instances of PCELLS in a layout can look totally different, as they can be bent round corners, meandered and the relative widths of different parts of the cell can be changed.

Figure 5 shows an example of a single transitor implemented in both types of cells.

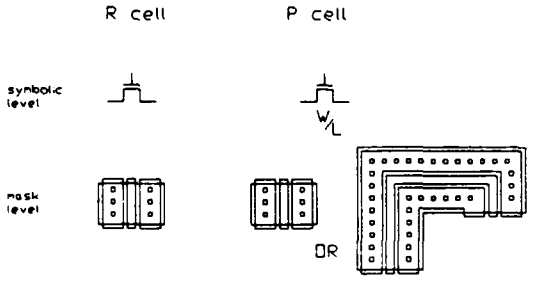

Figure 5 CustomPlus cells

9 Full custom Test Chip

We have made use of our research design facility to generate the mask pattern information for a full custom CMOS test chip. This was done to validate the design system and to evaluate some novel logic circuit elements being studied as part of our research. The layout data was sent to MCE on a magnetic tape and incorporated into one of the multiproject fabrication runs.

The final layout is shown in figure 6, as you can see from this there is an outer border of large bonding pads, the position and number of which is fixed for the chosen die size, but within this area there is total design freedom. The band of circuits within the bonding pads are a mixture of our logic circuit elements and input protection and output driver circuits. The central array of rectangles is a series of transistor test structures (incorporated by SP1) as part of a process characterisation program.

The devices were received in the 3rd quarter of 87 and initial evaluation of the chip has been very encouraging.

The design system works, the layout design rules have been successfully incorporated into the CustomPlus software. This has then been used to create working customised CMOS designs. The detailed design and simulation carried out for this chip along with an evaluation with be presented in a forthcoming RSRE memo.

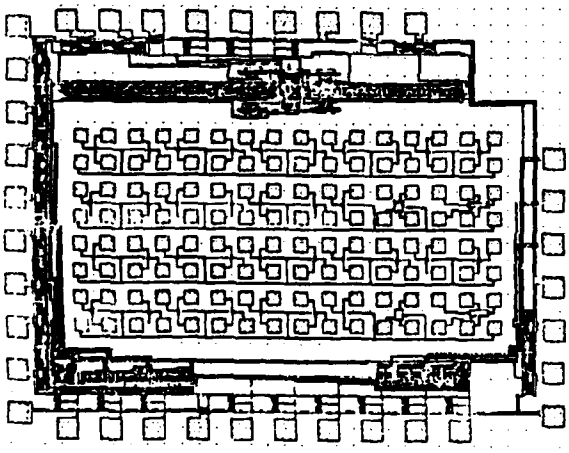

Figure 6 Test-chip layout

10 Conclusions

The very significant advantages that Custom ICs offer have been indicated and it has been shown that progress in Custom ICs has developed to the point where they must be considered by any designer contemplating PCB systems using even a few tens of standard logic ICs. The main classes of custom ICs have been detailed along with a guide to their applicability.

The design cycle and the levels of specification for Custom IC systems have been detailed.

It has been shown how a research full-custom facility has been set up and its effective use as part of our research program has been demonstrated.

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Abstract Customised or Application Specific ICs (ASICs) are being used increasingly as designers appreciate their benefits and its cost has reduced dramatically with the progress of CAD and processing technology. After a brief discussion of the benefits of the custom chip design route, the steps involved in the design cycle are outlined with particular emphasis on the practical aspects involved in translating circuit ideas to working silicon.

Shared-wafer silicon services have reduced significantly the cost of Full-custom chips and some practical experiences of Full Custom CMOS chip design are outlined. The design, simulation and layout were all carried out at RSRE. The work was undertaken as part of a research program on novel cell architectures for DSP VLSI chip design within SP2.

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